

What is claimed is:

1. A fuse circuit for adjusting an analog value, comprising:
 - a latch circuit which stores a setting state of a fuse element; and
 - 5 a latch clock generation circuit which generates a latch clock based on a cyclic signal, the latch clock being used for fetching the setting state of the fuse element into the latch circuit,
 - wherein the latch circuit cyclically fetches the setting state of the fuse element based on the latch clock, and
- 10 wherein the analog value is adjusted based on the setting state of the fuse element fetched by the latch circuit.
2. A fuse circuit for adjusting an analog value, comprising:
 - a plurality of latch circuits which store setting states of a plurality of fuse elements; and
 - 15 a latch clock generation circuit which generates a plurality of latch clocks of different phases corresponding to the respective latch circuits based on a cyclic signal,
 - wherein each of the latch circuits cyclically fetches the setting state of the corresponding one of the fuse elements based on the corresponding one of the latch
- 20 wherein the analog value is adjusted based on the setting states of the fuse elements fetched by the latch circuits.
3. The fuse circuit as defined in claim 2,
 - 25 wherein the latch clock generation circuit generates the latch clocks of different phases in units of a plural number of the latch circuits based on the cyclic signal.

4. The fuse circuit as defined in claim 2,
wherein the latch clocks are generated in synchronization with a rising edge and
a falling edge of the cyclic signal.

5. The fuse circuit as defined in claim 3,
wherein the latch clocks are generated in synchronization with a rising edge and
a falling edge of the cyclic signal.

6. The fuse circuit as defined in claim 1,
wherein the cyclic signal is a signal which changes for each frame.

7. The fuse circuit as defined in claim 2,
wherein the cyclic signal is a signal which changes for each frame.

8. The fuse circuit as defined in claim 3,
wherein the cyclic signal is a signal which changes for each frame.

9. The fuse circuit as defined in claim 4,
wherein the cyclic signal is a signal which changes for each frame.

10. The fuse circuit as defined in claim 5,
wherein the cyclic signal is a signal which changes for each frame.

11. The fuse circuit as defined in claim 1, further comprising:
a test signal holding circuit which holds a test signal for testing the setting state
of the fuse element;
a selector which selectively outputs one of the test signal held in the test signal

holding circuit and the setting state of the fuse element fetched by the latch circuit based on a select signal; and

a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clock,

5 wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of the fuse element fetched by the latch circuit when the latch clock is input.

12. The fuse circuit as defined in claim 2, further comprising:

10 a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

15 a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by corresponding one of the latch circuits when the latch clocks are input.

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13. The fuse circuit as defined in claim 3, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

25 a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

a select signal generation circuit which generates the select signal based on a test

mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by corresponding one of the latch circuits when the latch clocks are input.

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14. The fuse circuit as defined in claim 4, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

10 a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

15 a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the

15 selector selectively outputs the setting state of each of the fuse elements fetched by corresponding one of the latch circuits when the latch clocks are input.

15. The fuse circuit as defined in claim 5, further comprising:

20 a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

25 a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by

corresponding one of the latch circuits when the latch clocks are input.

16. The fuse circuit as defined in claim 6, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state
5 of the fuse element;

a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of the fuse element fetched by the latch circuit based on a select signal; and

10 a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clock,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of the fuse element fetched by the latch circuit when the latch clock is input.

15 17. The fuse circuit as defined in claim 7, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by
20 corresponding one of the latch circuits based on a select signal; and

a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by
25 corresponding one of the latch circuits when the latch clocks are input.

18. The fuse circuit as defined in claim 8, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by 5 corresponding one of the latch circuits based on a select signal; and

a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by 10 corresponding one of the latch circuits when the latch clocks are input.

19. The fuse circuit as defined in claim 9, further comprising:

a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

15 a selector which selectively outputs one of the test signal held in the test signal holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

20 wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by corresponding one of the latch circuits when the latch clocks are input.

20. The fuse circuit as defined in claim 10, further comprising:

25 a test signal holding circuit which holds a test signal for testing the setting state of each of the fuse elements;

a selector which selectively outputs one of the test signal held in the test signal

holding circuit and the setting state of each of the fuse elements fetched by corresponding one of the latch circuits based on a select signal; and

a select signal generation circuit which generates the select signal based on a test mode setting signal and the latch clocks,

5 wherein the select signal generation circuit generates the select signal so that the selector selectively outputs the setting state of each of the fuse elements fetched by corresponding one of the latch circuits when the latch clocks are input.

21. A display driver circuit comprising:

10 the fuse circuit as defined in claim 1; and

 a driver circuit which drives a display panel based on a voltage value or a current value adjusted by the fuse circuit and based on the cyclic signal.

22. A display driver circuit comprising:

15 the fuse circuit as defined in claim 2; and

 a driver circuit which drives a display panel based on a voltage value or a current value adjusted by the fuse circuit and based on the cyclic signal.

23. A display driver circuit comprising:

20 the fuse circuit as defined in claim 11; and

 a driver circuit which drives a display panel based on a voltage value or a current value adjusted by the fuse circuit and based on the cyclic signal.

24. A display driver circuit comprising:

25 the fuse circuit as defined in claim 12; and

 a driver circuit which drives a display panel based on a voltage value or a current value adjusted by the fuse circuit and based on the cyclic signal.

25. The fuse circuit as defined in claim 1,
wherein the analog value is a current value, voltage value, or oscillation
frequency.

5 26. The fuse circuit as defined in claim 2,
wherein the analog value is a current value, voltage value, or oscillation
frequency.

10 27. The display driver circuit as defined in claim 21,
wherein the analog value is a current value in the display driver circuit, voltage
value in the display driver circuit, or oscillation frequency in the display driver circuit.

15 28. The display driver circuit as defined in claim 22,
wherein the analog value is a current value in the display driver circuit, voltage
value in the display driver circuit, or oscillation frequency in the display driver circuit.

20 29. The display driver circuit as defined in claim 23,
wherein the analog value is a current value in the display driver circuit, voltage
value in the display driver circuit, or oscillation frequency in the display driver circuit.

25 30. The display driver circuit as defined in claim 24,
wherein the analog value is a current value in the display driver circuit, voltage
value in the display driver circuit, or oscillation frequency in the display driver circuit.